AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

Listing of Claims:

Claims 1-67 (Canceled).

Claim 68 (Currently Amended): A method of assembling a first wafer onto a second wafer, the first wafer including a lower layer having no circuits and components, and an upper transplant layer arranged at least under the frontal side of the first wafer, the transplant layer having~~that has~~ at least one of circuits and components, comprising:

eliminating material from the ~~first wafer having the~~ upper transplant layer and the lower layer from a frontal side of the first wafer in a peripheral area of the first wafer~~, the transplant layer arranged at least under the frontal side of the first wafer~~, over a thickness less than ~~a~~ an entire thickness of the first wafer, but greater than ~~a~~ an entire thickness of the upper transplant layer, after the at least one of circuits and components have been formed in the upper transplant layer; and

assembling the upper transplant layer of the first wafer onto a second wafer after said eliminating material.

Claim 69 (Withdrawn): A method as in claim 68, wherein the first wafer previously is covered with a protective layer.

Claim 70 (Withdrawn): A method as in claim 69, wherein the protective layer is eliminated locally, before routing the first waver, in a zone located above a zone to be routed of the first wafer.

Claim 71 (Withdrawn): A method as in claim 70, wherein the local elimination of the protective layer is performed via lithography and etching.

Claim 72 (Withdrawn): A method as in claim 69, wherein the protective layer is eliminated after routing the first wafer.

Claim 73 (Cancelled).

Claim 74 (Previously Presented): A method as in claim 68, wherein the first wafer is chamfered and includes at least a chamfered edge.

Claim 75 (Previously Presented): A method as in claim 74, wherein the eliminating is performed over a width, measured on a plane parallel to the frontal side of the first wafer, at least equal to a width of the chamfered edge, measured on the same plane.

Claim 76 (Previously Presented): A method as in claim 68, further comprising:

additional eliminating of material after said assembling of the first and second wafers.

Claim 77 (Previously Presented): A method as in claim 68, wherein the eliminating is performed over a thickness of the first wafer between 1 μm and 100 μm.

Claim 78 (Previously Presented): A method as in claim 68, wherein the eliminating is performed over a width, measured on a plane parallel to the frontal side of the first wafer, at least equal to a width of a zone of the first wafer which can not, without said step of eliminating, be assembled with the second wafer.

Claim 79 (Previously Presented): A method as in claim 68, wherein the eliminating is performed over a width, measured on a plane parallel to the frontal side of the first wafer of between 100 μm and 5 mm.

Claims 80-84 (Cancelled).

Claim 85 (Previously Presented): A method as in claim 68, wherein the assembling the first and second wafers is performed via molecular adhesion or via bonding using an adhesive substance.

Claim 86 (Cancelled).

Claim 87 (Previously Presented): A method as in claim 68, wherein the eliminating takes place after a previous surface preparation of the first wafer for a purpose of assembling.

Claim 88 (Previously Presented): A method as in claim 68, wherein the eliminating takes place before a previous surface penetration of the first wafer for a purpose of assembling.

Claim 89 (Previously Presented): A method as in claim 68, wherein the eliminating is performed via mechanical or chemical or mechano-chemical etching or polishing or via plasma etching or via a combination of at least two of these types of etching.

Claim 90 (Previously Presented): A method as in claim 68, wherein at least one of

the first and the second wafers is made in a semiconductor material.

Claim 91 (Previously Presented): A method as in claim 68, wherein at least one of the first and the second wafers is made in silicon or in a III-V type semiconductor material.

Claim 92 (Previously Presented): A method as in claim 68, wherein at least one of the first and the second wafers is made in Germanium or in Germanium silicide (SiGe) or in a piezoelectric material or in an insulating material.

Claim 93 (Previously Presented): A method as in claim 68, wherein the eliminating is performed in a regular manner around the first wafer.

Claims 94-97 (Cancelled).

Claim 98 (Currently Amended): A method as in claim 68, further comprising:

additional eliminating of material from the first wafer from a lateral side of the first wafer over a length L_2 that removes some material of the upper transplant layer.